UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,562	11/24/2003	Anthony Correale JR.	YOR920030359US1	5731

33233 7590 11/23/2005

LAW OFFICE OF CHARLES W. PETERSON, JR.
11703 BOWMAN GREEN DRIVE
SUITE 100
RESTON, VA 20190

EXAMINER	
GARBOWSKI, LEIGH M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/720,562	CORREALE ET AL.
	Examiner	Art Unit
	Leigh Marie Garbowski	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,10,11,14,16,18,19,24,26,31,35,36 and 38* is/are rejected.

7)☒ Claim(s) *1-5,7-9,12,13,15,17,20-30,32-34 and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892) 2 sheets

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/24/2003*. 2 sheets

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

Specification

The disclosure is objected to because of the following informalities: the cross reference information must be updated and the attorney docket numbers must deleted throughout the specification.

Appropriate correction is required.

Claim Objections

Claims 1, 4, 22, 26 are objected to because of the following informalities: as per claim 1, the antecedent basis for "each level converter" [line 3] is not clear; since step b) provides for plural "level converters" [line 7], the scope of the method is not clear; as per claim 4, "in claim 1 at least" [line 1] is confusing; as per claim 22, "wherein, wherein" [line 1] is confusing; as per claim 26, since there is no antecedent basis for "locating said side drive point" [line 1], language should be inserted to provide for the method further comprising such a locating step. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 6, 11, 14, 16, 18, 19, 24, 26, 35, 36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 6 and 24, there is no antecedent basis for "said minimum distance" [line 1], thus what is meant by locating is not clear. As per claim 11, there is no antecedent basis for "level converter fanin cones" [line 2], thus what is meant by

deleting is not clear. As per claim 14, what is meant by "second voltage level circuit elements" [line 3] is confusing, where or what are "first" voltage level circuit elements? As per claim 16, there is no antecedent basis for "first voltage level buffer" [line 2], thus what is meant by replacing is not clear. As per claim 18, the antecedent basis for "placing and wiring step (a)" [line 2] is confusing. As per claim 19, there is no antecedent basis for "level converter fanin cones" [line 10], thus what is meant by deleting is not clear; what is meant by "second voltage level circuit elements" [line 12] is confusing, where or what are "first" voltage level circuit elements? Also, there is no antecedent basis for "first voltage level buffer" [line 15], thus what is meant by replacing is not clear. As per claim 35, there is no antecedent basis for "level converter fanin cones" [lines 3-4], thus what is meant by identifying and deleting is not clear. As per claim 36, there is no antecedent basis for "the computer program code means for locating said identifying and deleting" [lines 1-2], thus rendering the claim vague and indefinite.

The following rejections are based on the examiner's best interpretation in view of the issues raised above.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 10, 18, 31, 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al. ["On Gate Level Power Optimization Using Dual-Supply Voltages"].

As per claim 1, a method of optimizing level converter placement, comprising: a) selectively placing each level converter at a minimum power point to minimize net power and transitional delay, transitional delay being a first voltage net delay to said level converter, through said level converter and a second voltage net delay from said level converter [section IV.]; and b) eliminating inefficient level converters [Abstract; section V.]. As per claim 10, wherein at said minimum power point is selected to minimize wiring [section II., last paragraph]. As per claim 18, wherein and input netlist, technology definition and timing constraints are provided for [figure 2].

As per claim 31, a computer program product for optimizing level converter placement in a multi-supply IC design, comprising: computer program code means for locating a minimum power point to minimize power and transitional delay for a level converter placed at said minimum power point, transitional delay being a first voltage net delay to said level converter, through said level converter and a second voltage net delay from said level converter [section IV.]; computer program code means for placing level converters at minimum power points [section V.]; and computer program code means for eliminating inefficient said level converters [Abstract; section V.]. As per claim 38, further comprising: computer program code means for receiving an input netlist, technology definition and timing constraints [figure 2].

Claims 1, 10, 18, 31, 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Igarashi et al. ["A Low-power Design Method Using Multiple Supply Voltages"].

As per claim 1, a method of optimizing level converter placement, comprising: a) selectively placing each level converter at a minimum power point to minimize net power and transitional delay, transitional delay being a first voltage net delay to said level converter, through said level converter and a second voltage net delay from said level converter [sections 3 and 5]; and b) eliminating inefficient level converters [section 5]. As per claim 10, wherein at said minimum power point is selected to minimize wiring [Abstract; section 5]. As per claim 18, wherein and input netlist, technology definition and timing constraints are provided for [figure 1].

As per claim 31, a computer program product for optimizing level converter placement in a multi-supply IC design, comprising: computer program code means for locating a minimum power point to minimize power and transitional delay for a level converter placed at said minimum power point, transitional delay being a first voltage net delay to said level converter, through said level converter and a second voltage net delay from said level converter [sections 3 and 5]; computer program code means for placing level converters at minimum power points [sections 3 and 5]; and computer program code means for eliminating inefficient said level converters [section 5]. As per claim 38, further comprising: computer program code means for receiving an input netlist, technology definition and timing constraints [figure 1].

Claims 1, 10, 18, 31, 38 are rejected under 35 U.S.C. 102(a) as being anticipated by Kang et al. ["Multiple-Vdd Scheduling/Allocation for Partitioned Floorplan"].

As per claim 1, a method of optimizing level converter placement, comprising: a) selectively placing each level converter at a minimum power point to minimize net

power and transitional delay, transitional delay being a first voltage net delay to said level converter, through said level converter and a second voltage net delay from said level converter [Abstract; section 2]; and b) eliminating inefficient level converters [Abstract; section 3]. As per claim 10, wherein at said minimum power point is selected to minimize wiring [Abstract]. As per claim 18, wherein and input netlist, technology definition and timing constraints are provided for [figures 3 and 4].

As per claim 31, a computer program product for optimizing level converter placement in a multi-supply IC design, comprising: computer program code means for locating a minimum power point to minimize power and transitional delay for a level converter placed at said minimum power point, transitional delay being a first voltage net delay to said level converter, through said level converter and a second voltage net delay from said level converter [Abstract; section 2]; computer program code means for placing level converters at minimum power points [Abstract; section 2]; and computer program code means for eliminating inefficient said level converters [Abstract; section 3]. As per claim 38, further comprising: computer program code means for receiving an input netlist, technology definition and timing constraints [figures 3 and 4].

Allowable Subject Matter

Claim 19 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Claims 20-30 are objected to as being dependent upon a rejected base claim.

Claims 6, 11, 14, 16, 35, 36 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claims 2-5, 7-9, 12-13, 15, 17, 32-34, 37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-FORM 892.Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leigh Marie Garbowski whose telephone number is 571-272-1893 and e-mail is Leigh.Garbowski@uspto.gov. The examiner can normally be reached on days.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LEIGH M. GARBOWSKI
PRIMARY EXAMINER